Notice of Allowability	Application No.	Applicant(s)	
	10/022,428	MATSUSHIMA, YUSUKE	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 09/21/04*.

2. ☒ The allowed claim(s) is/are *1 and 2*.

3. ☒ The drawings filed on *20 December 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

1. Claims 1 and 2 have been examined. Claims 3-6 have been canceled.

Response to Arguments

1. Applicant's arguments, see Applicant Remarks, filed September 21, 2004, with respect to claims 1 and 2 have been fully considered and are persuasive. The Examiner has withdrawn the rejection of claims 1-2 as a result of Applicant's amendment of September 21, 2004.

Allowable Subject Matter

2. Claims 1-2 are allowed.

The following is an Examiner's Statement of Reason for Allowance.

The present invention relates to a scanning flip-flop circuit for use as a flip-flop circuit in testing a semiconductor integrated circuit device.

The claimed invention as set forth in claim 1 recites features such as: **a master latch and a slave latch** each for temporarily holding an input signal; **a first scan controller** for receiving an output signal from said master latch and outputting the received output signal in synchronism with a scan clock which is a clock for testing the semiconductor integrated circuit device, when the semiconductor integrated circuit device is tested; **a clock controller** for receiving an output signal from said first scan controller and outputting the received output signal to said slave unit in synchronism

with a predetermined clock when in a normal mode of operation; and **a second scan controller** having an input terminal connected to an output terminal of said first scan controller, for outputting a scan-out signal corresponding to a scan-in signal which is an input signal for testing the semiconductor integrated circuit device, in synchronism with said scan clock when the semiconductor integrated circuit device is tested..

The prior art of record teaches a master latch and a slave latch; a clock controller; and a second scan controller; Zasio et al. (US-4495629) is an example of such prior art. The prior arts of record, however, fail to teach, singly or in combination, a first scan controller as recited in claim 1. As such, modification of the prior art of record to include the claimed first scan controller can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the first scan controller set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the first scan controller.

The Examiner agrees with the Applicant's arguments with regard to these features in view of the arts of record; therefore, the Examiner favors the allowance of claims 1-2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

5/10/05

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